

Reed-Solomon Block Encoder/Decoder on a soft-core CPU

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ABSTRACT

This paper describes the process of porting an existing Reed-Solomon encoder and decoder to a soft-core CPU, and also attempts to find a way to convert the C code of each into Verilog, which can be synthesised and programmed onto an FPGA. The paper shows how the first goal is realised, and the performance of the encoder and decoder is tested. It goes on to show how the second goal is only partially realised, limited – in the cases of both encoder and decoder – by the available tooling and the programming methodology behind the source code. It ends considering how this process could be simplified.

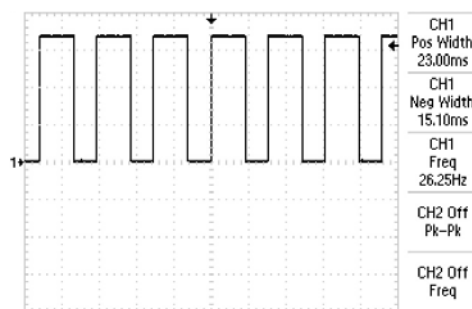


Figure 1: Reed-Solomon decoder output timing trace

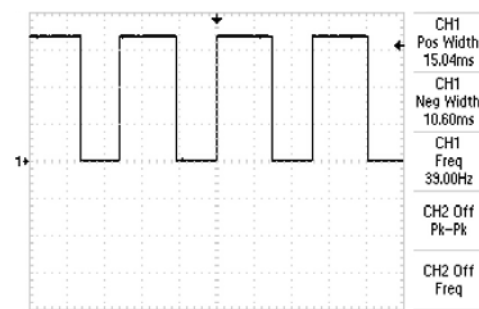


Figure 3: Reed-Solomon encoder output timing trace

D Salisbury, Reed-Solomon Block Encoder/Decoder on a soft-core CPU, *Proc. 11th School Conf. for Annual Research Projects*, V F Ruiz (Ed), pp. 431–434, University of Reading, 29 May 2012.